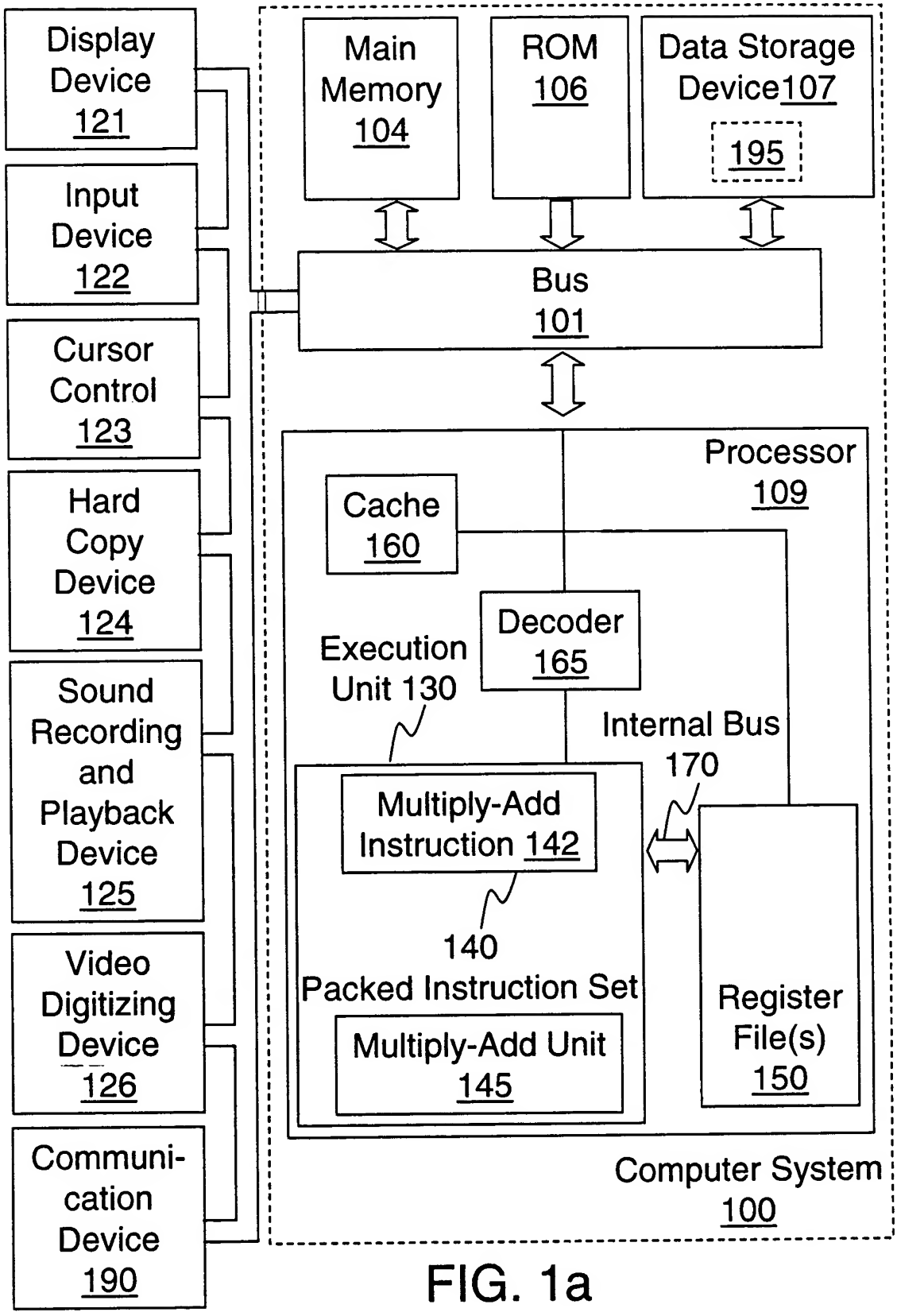

Display Device 121
Input Device 122
Cursor Control 123
Hard Copy Device 124
Sound Recording and Playback Device 125
Video Digitizing Device 126
Communi-cation Device 190
Main Memory 104
ROM 106
Data Storage Device 107
195
Bus 101
Processor 109
Cache 160
Decoder 165
Execution Unit 130
Internal Bus 170
Multiply-Add Instruction 142
140
Packed Instruction Set
Multiply-Add Unit 145
Register File(s) 150
Computer System 100

FIG. 1a

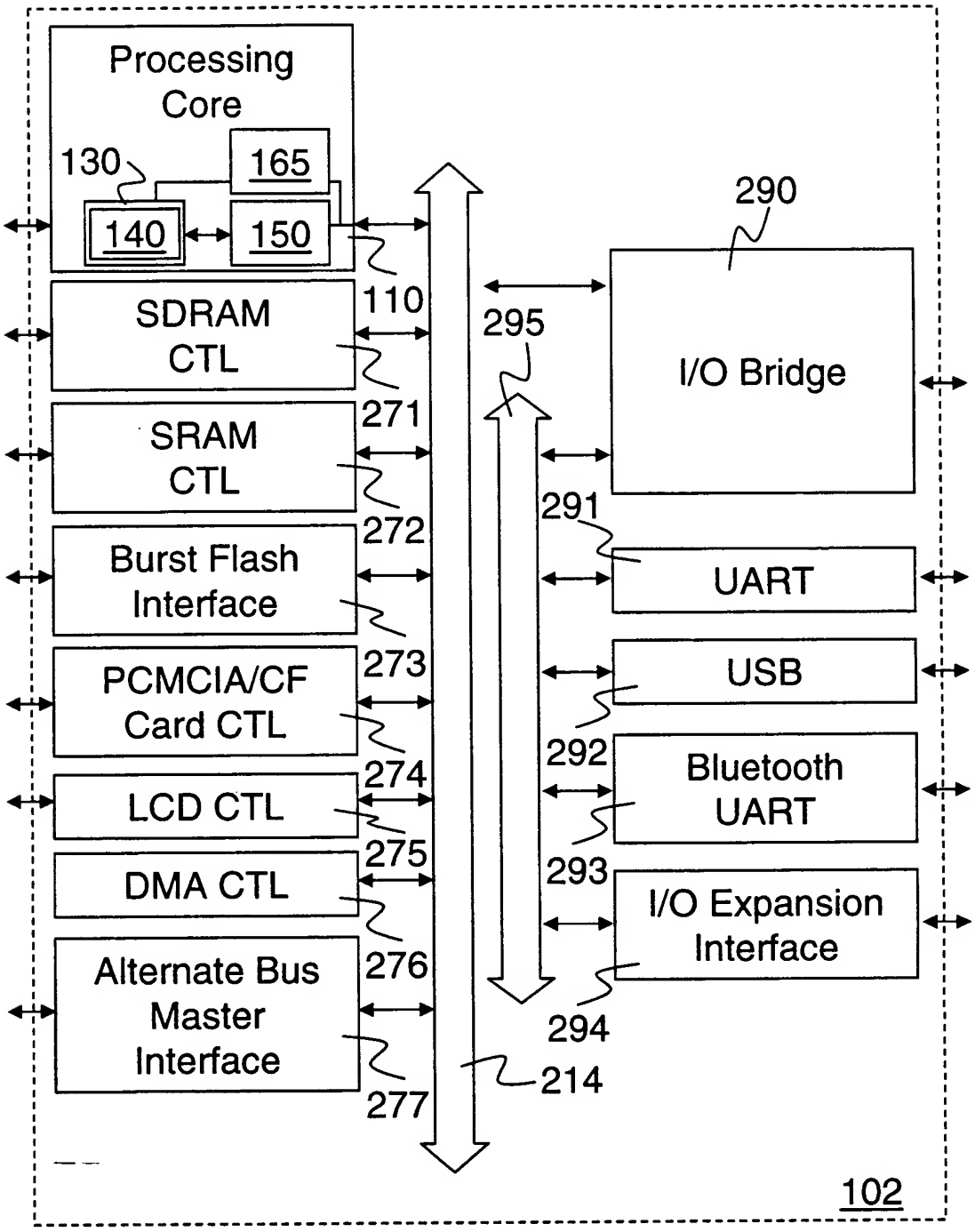

Processing Core
130
165
140
150
SDRAM CTL
110
SRAM CTL
271
Burst Flash Interface
272
PCMCIA/CF Card CTL
273
LCD CTL
274
DMA CTL
275
Alternate Bus Master Interface
276
277
295
290
I/O Bridge
291
UART
USB
292
Bluetooth UART
293
I/O Expansion Interface
294
214
102

FIG. 1b

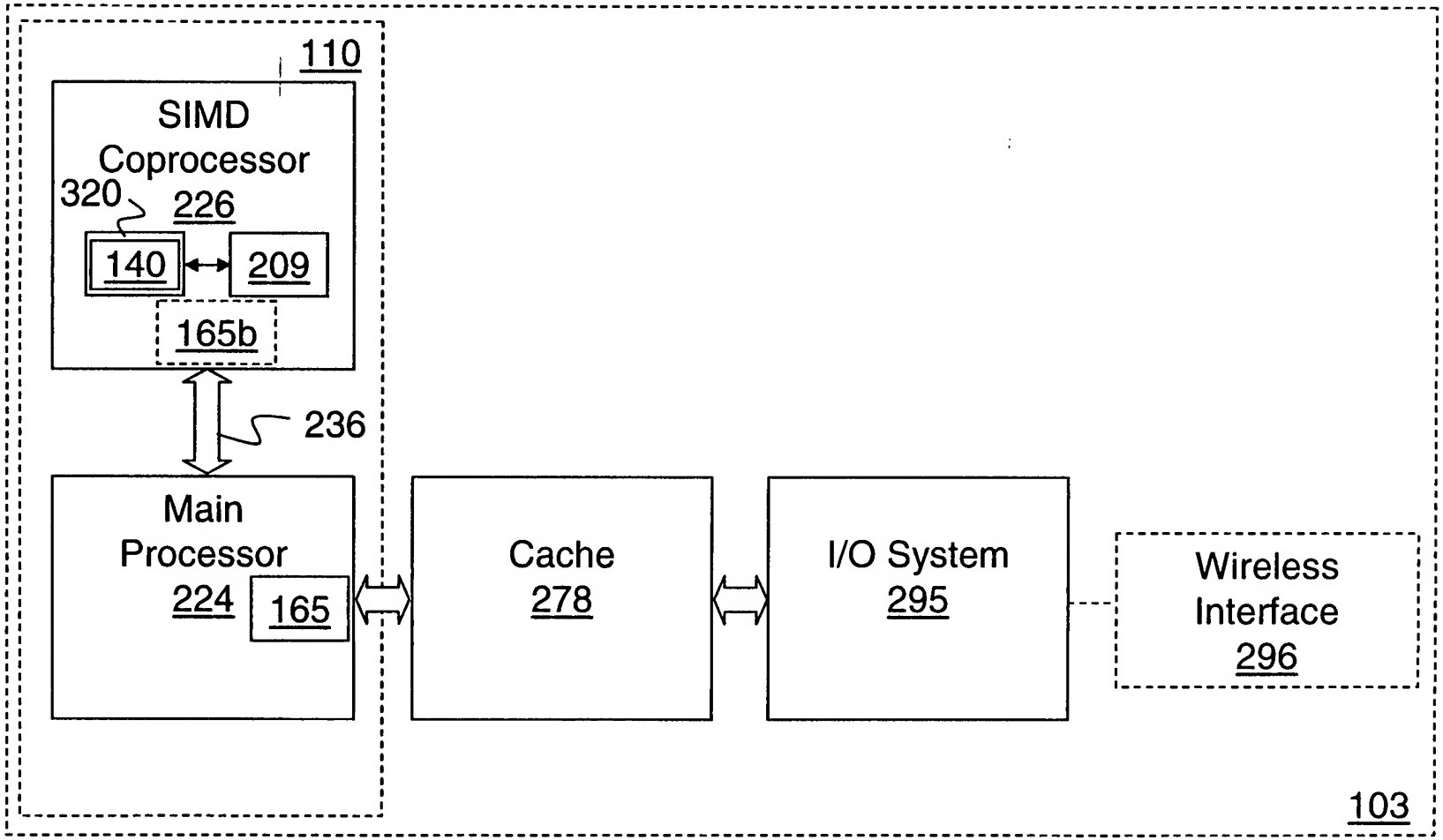

110
SIMD
Coprocessor
320
226
140
209
165b
236
Main
Processor
224
165
Cache
278
I/O System
295
Wireless
Interface
296
103

FIG. 1c

FIG. 2a

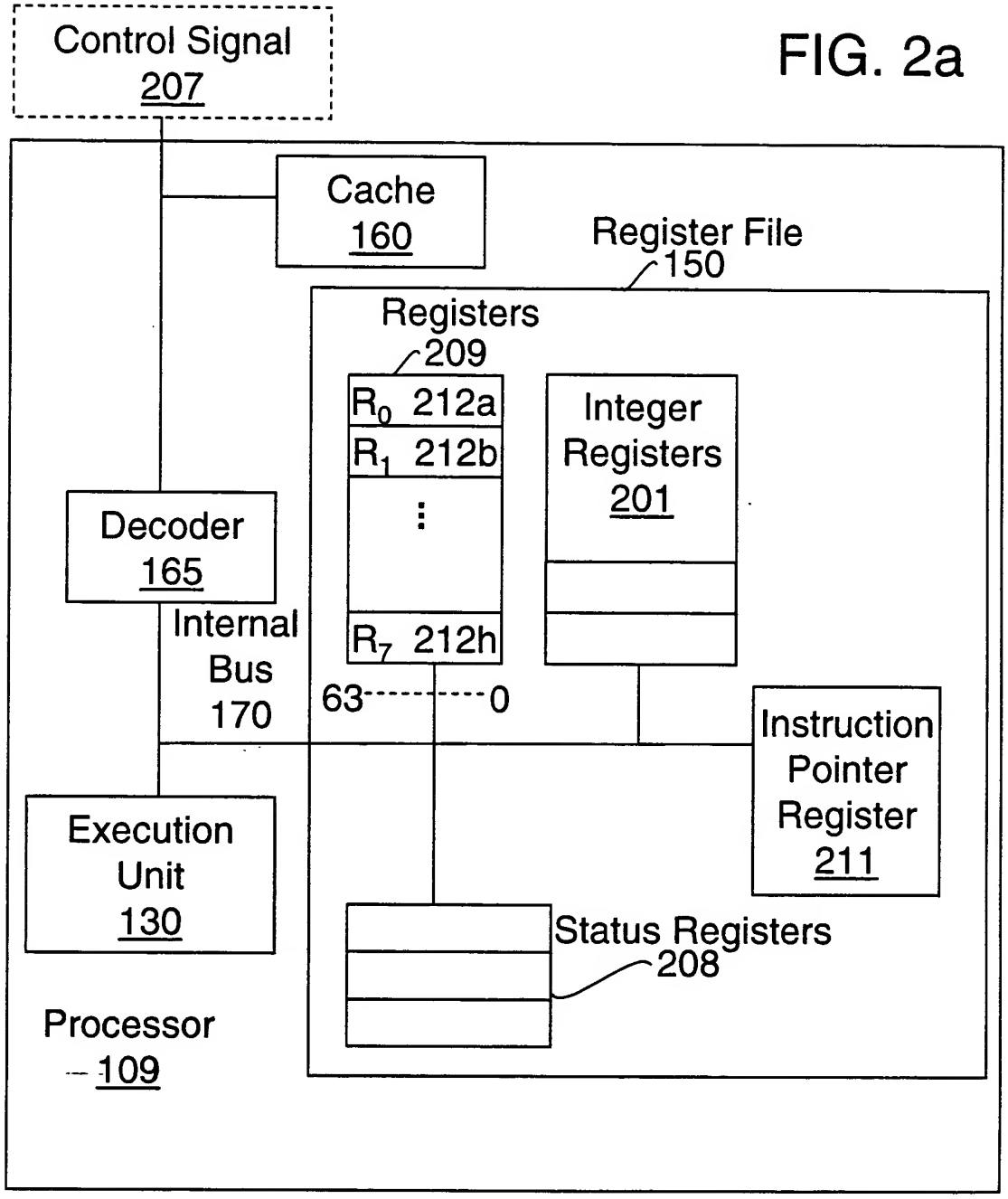

Control Signal
207
Cache
160
Register File
150
Registers
209
R_0 212a
R_1 212b
R_7 212h
Integer
Registers
201
Decoder
165
Internal
Bus
170
63
0
Instruction
Pointer
Register
211
Execution
Unit
130
Status Registers
208
Processor
109

FIG. 2b

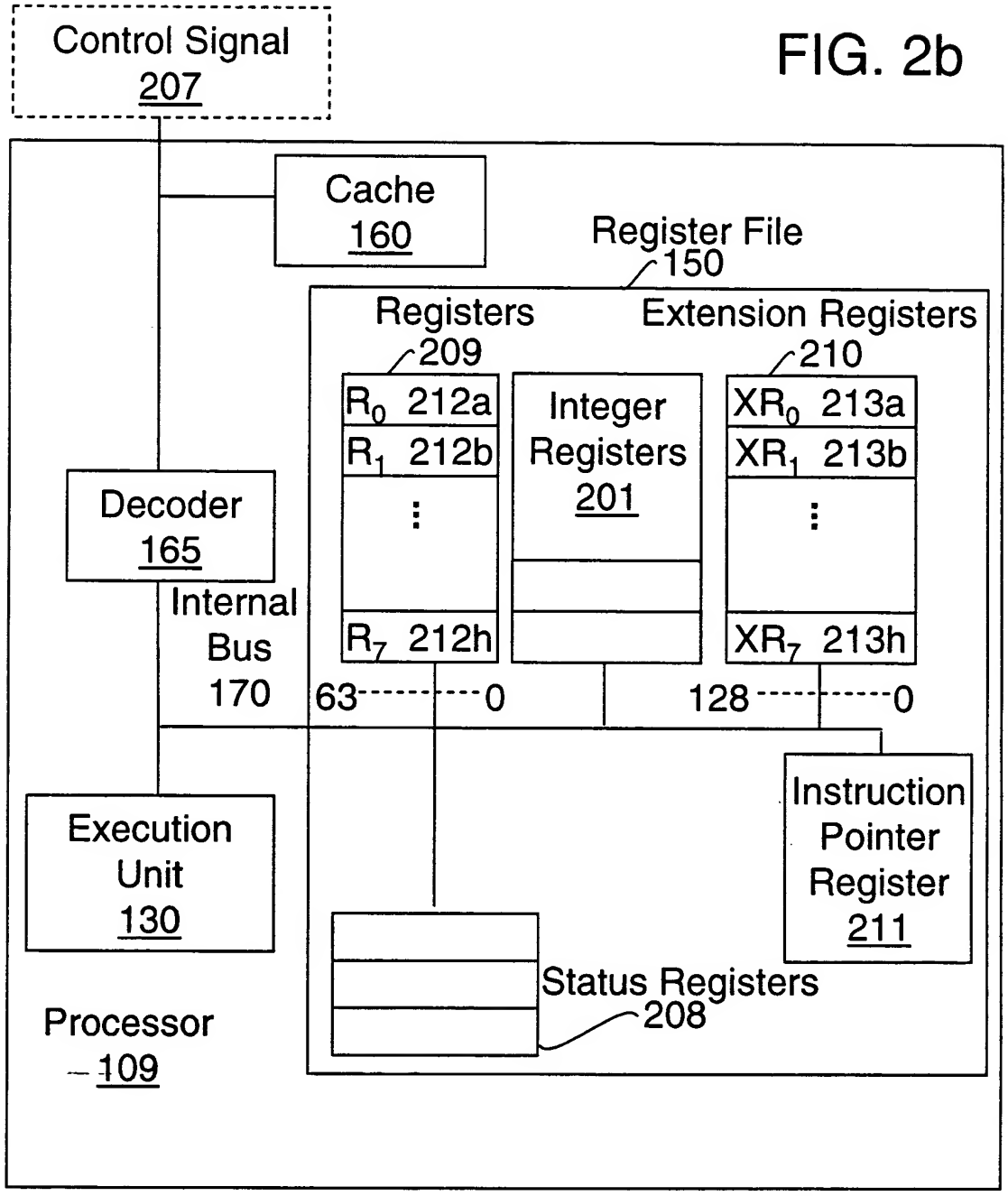
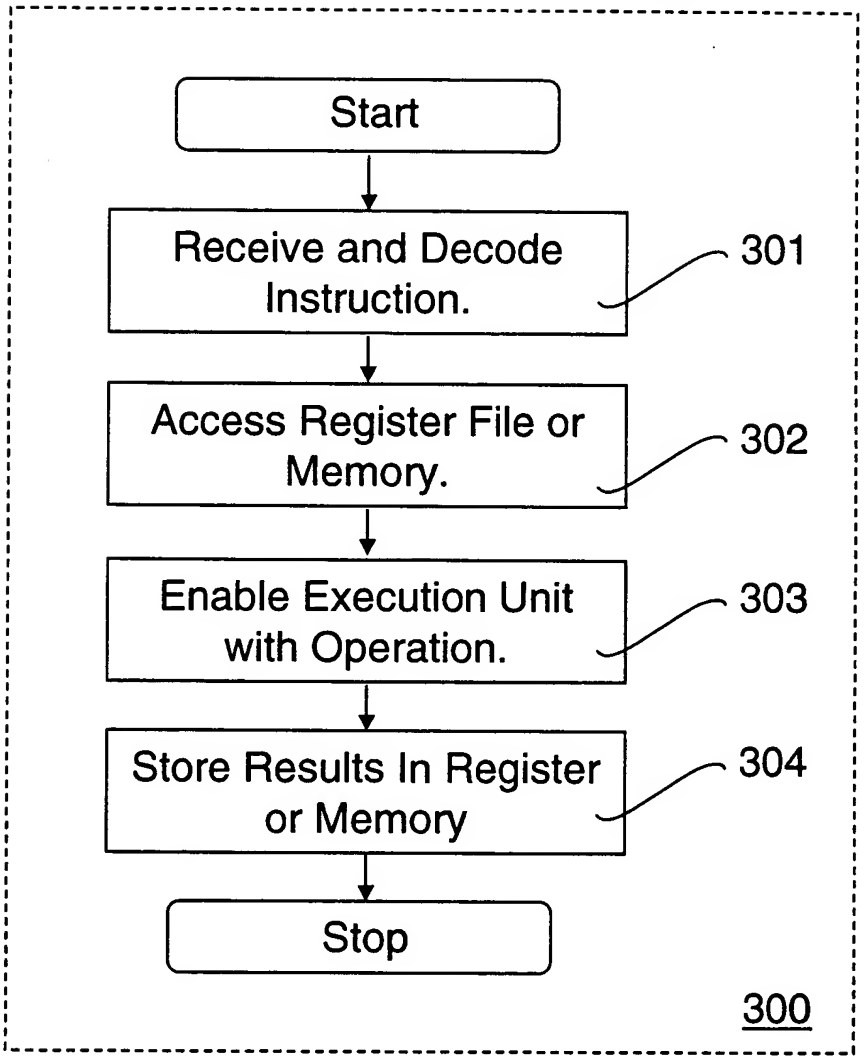

Control Signal
207
Cache
160
Register File
150
Registers
209
Extension Registers
210
R_0 212a
R_1 212b
R_7 212h
Integer
Registers
201
XR_0 213a
XR_1 213b
XR_7 213h
Decoder
165
Internal
Bus
170
63
0
128
0
Execution
Unit
130
Instruction
Pointer
Register
211
Status Registers
208
Processor
109

FIG. 3


Start
Receive and Decode Instruction.
301
Access Register File or Memory.
302
Enable Execution Unit with Operation.
303
Store Results In Register or Memory
304
Stop
300

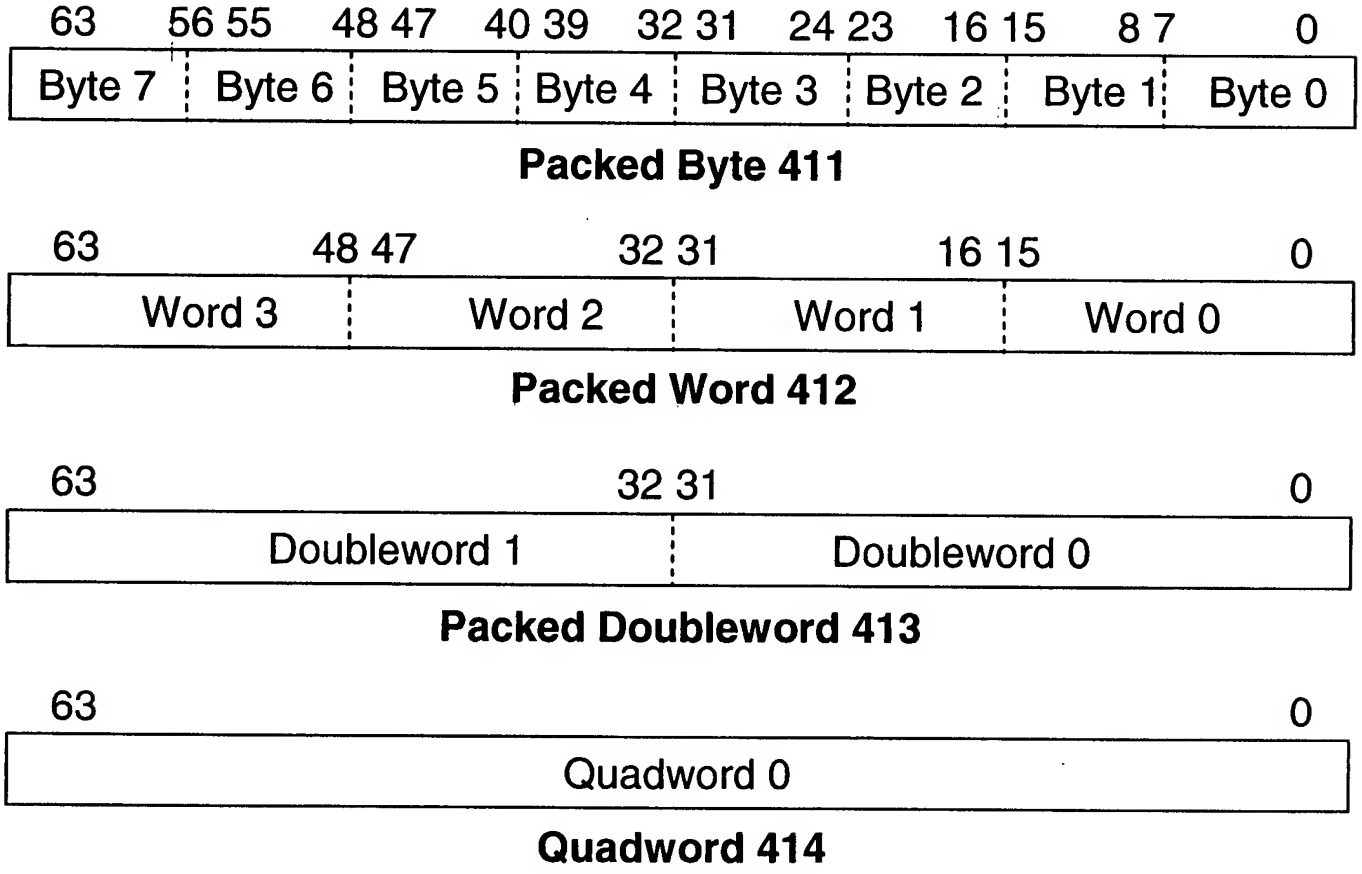

63 56 55 48 47 40 39 32 31 24 23 16 15 8 7 0
Byte 7
Byte 6
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Packed Byte 411
63 48 47 32 31 16 15 0
Word 3
Word 2
Word 1
Word 0
Packed Word 412
63 32 31 0
Doubleword 1
Doubleword 0
Packed Doubleword 413
63 0
Quadword 0
Quadword 414

FIG. 4a

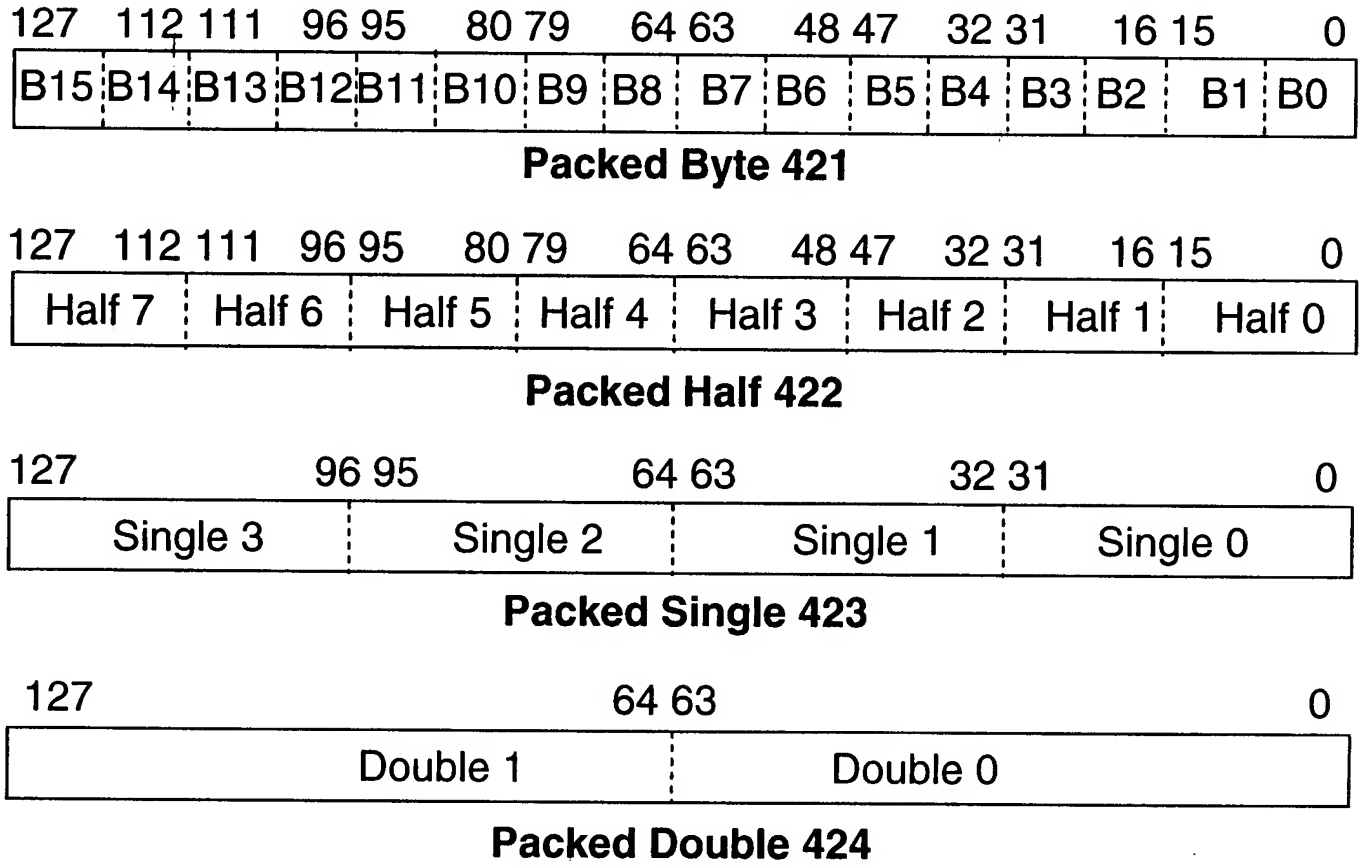
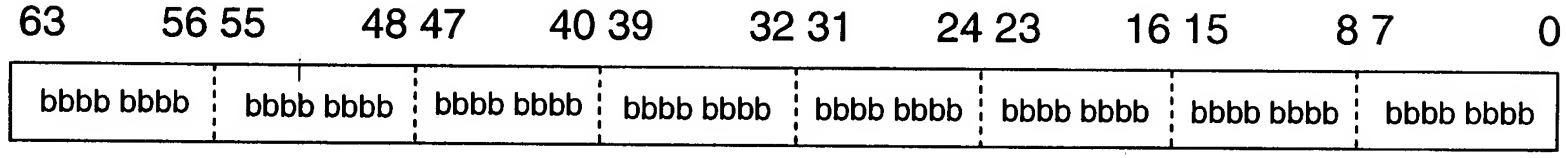
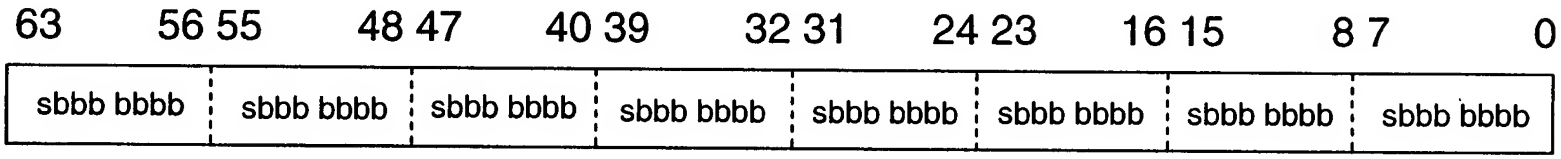

127 112 111 96 95 80 79 64 63 48 47 32 31 16 15 0
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
Packed Byte 421
127 112 111 96 95 80 79 64 63 48 47 32 31 16 15 0
Half 7 Half 6 Half 5 Half 4 Half 3 Half 2 Half 1 Half 0
Packed Half 422
127 96 95 64 63 32 31 0
Single 3 Single 2 Single 1 Single 0
Packed Single 423
127 64 63 0
Double 1 Double 0
Packed Double 424

FIG. 4b

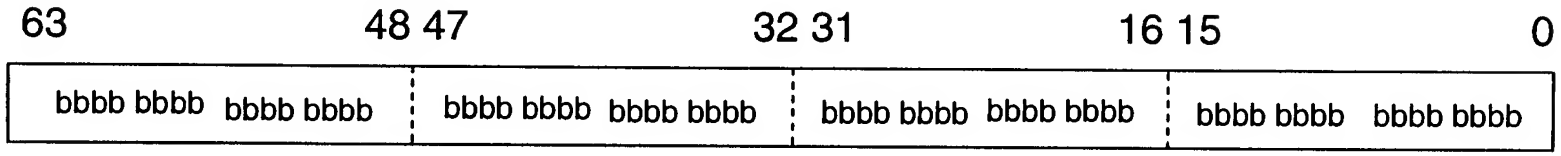


Unsigned packed byte in-register representation 510

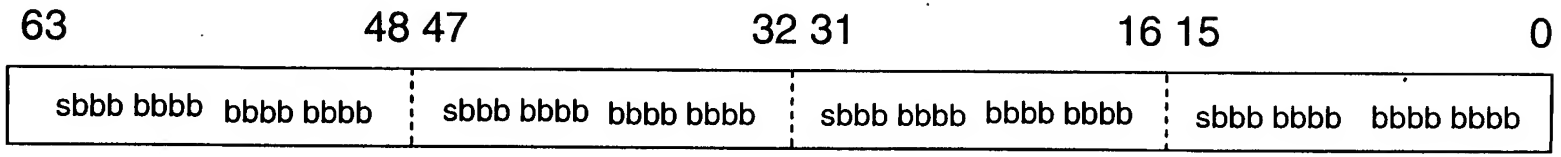


Signed packed byte in-register representation 511

FIG. 5a

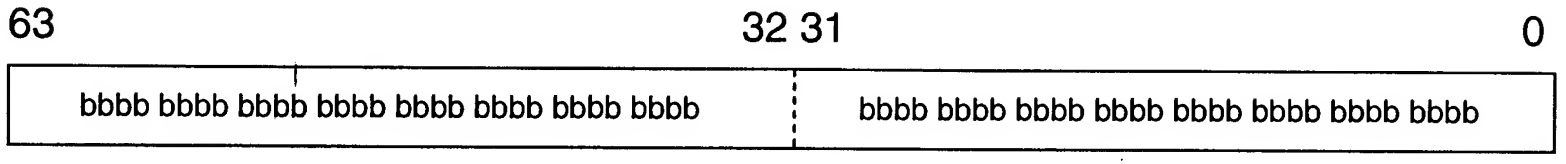


Unsigned packed word in-register representation 512

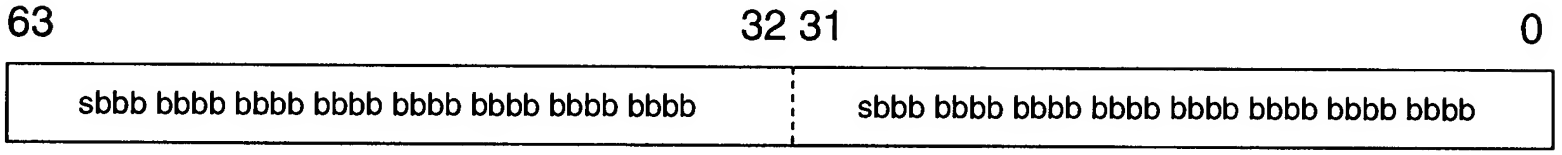


Signed packed word in-register representation 513

FIG. 5b

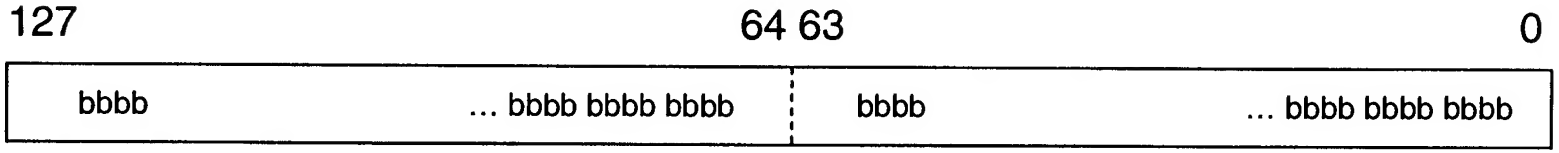


Unsigned packed doubleword in-register representation 514

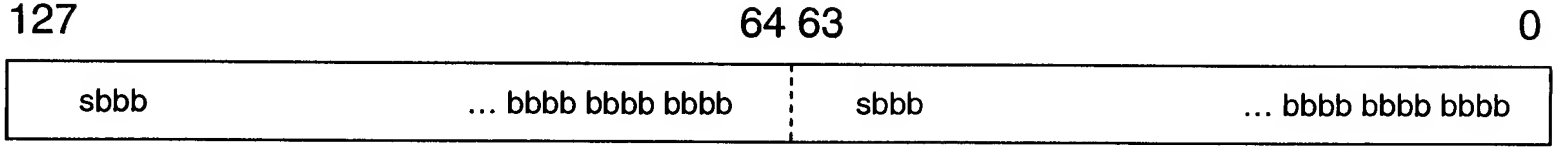


Signed packed doubleword in-register representation 515

FIG. 5c



Unsigned packed quadword in-register representation 516



Signed packed quadword in-register representation 517

FIG. 5d

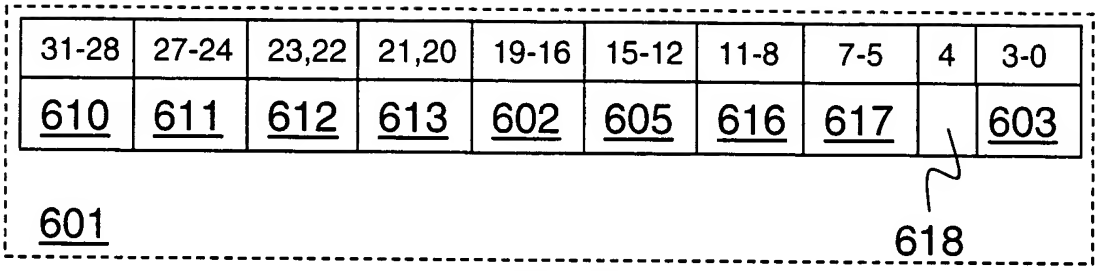


FIG. 6a

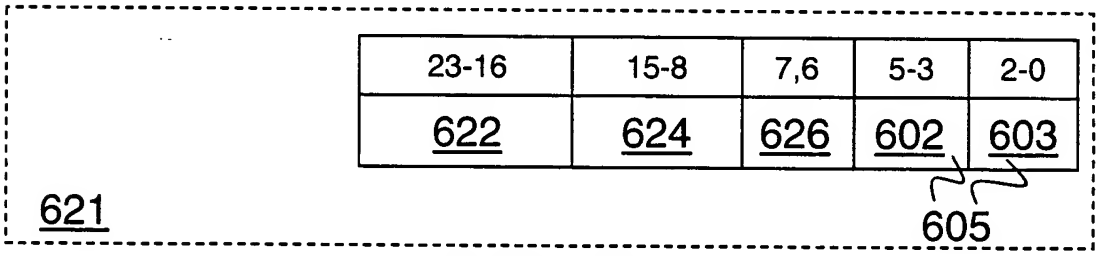


FIG. 6b

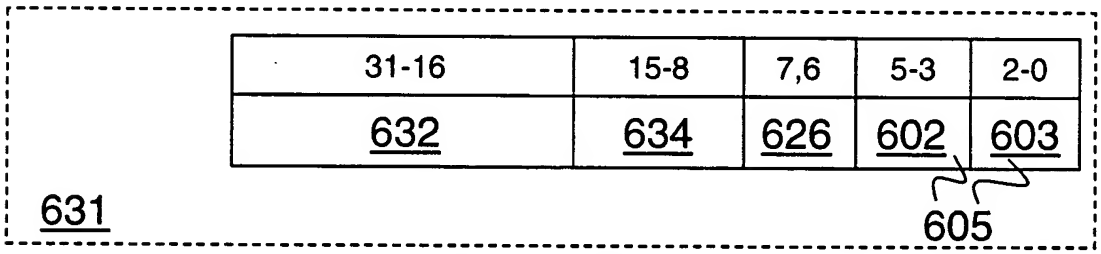


FIG. 6c

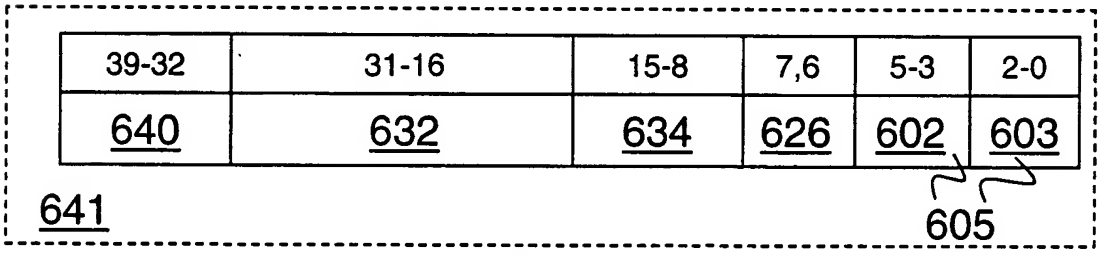


FIG. 6d

FIG. 7a

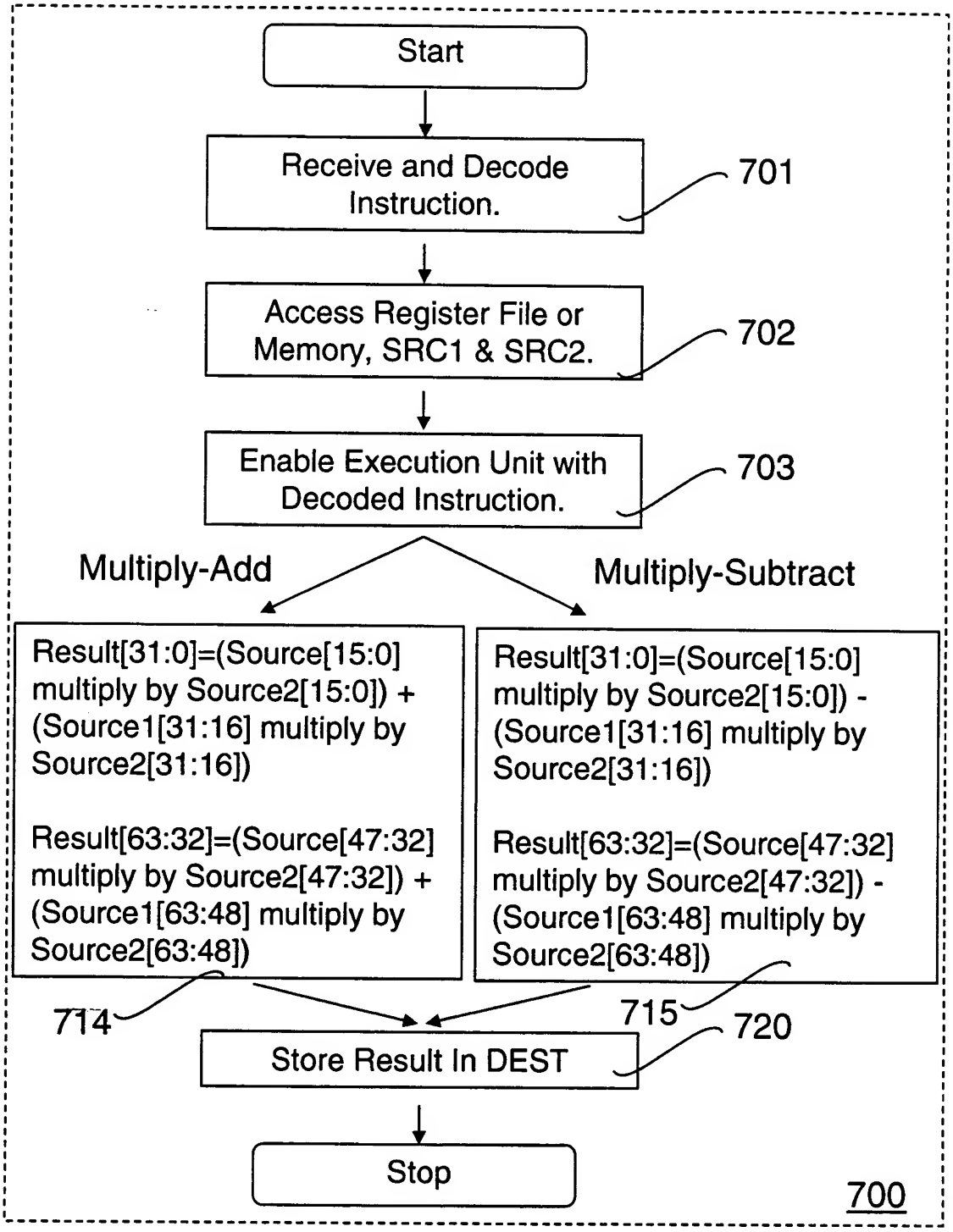
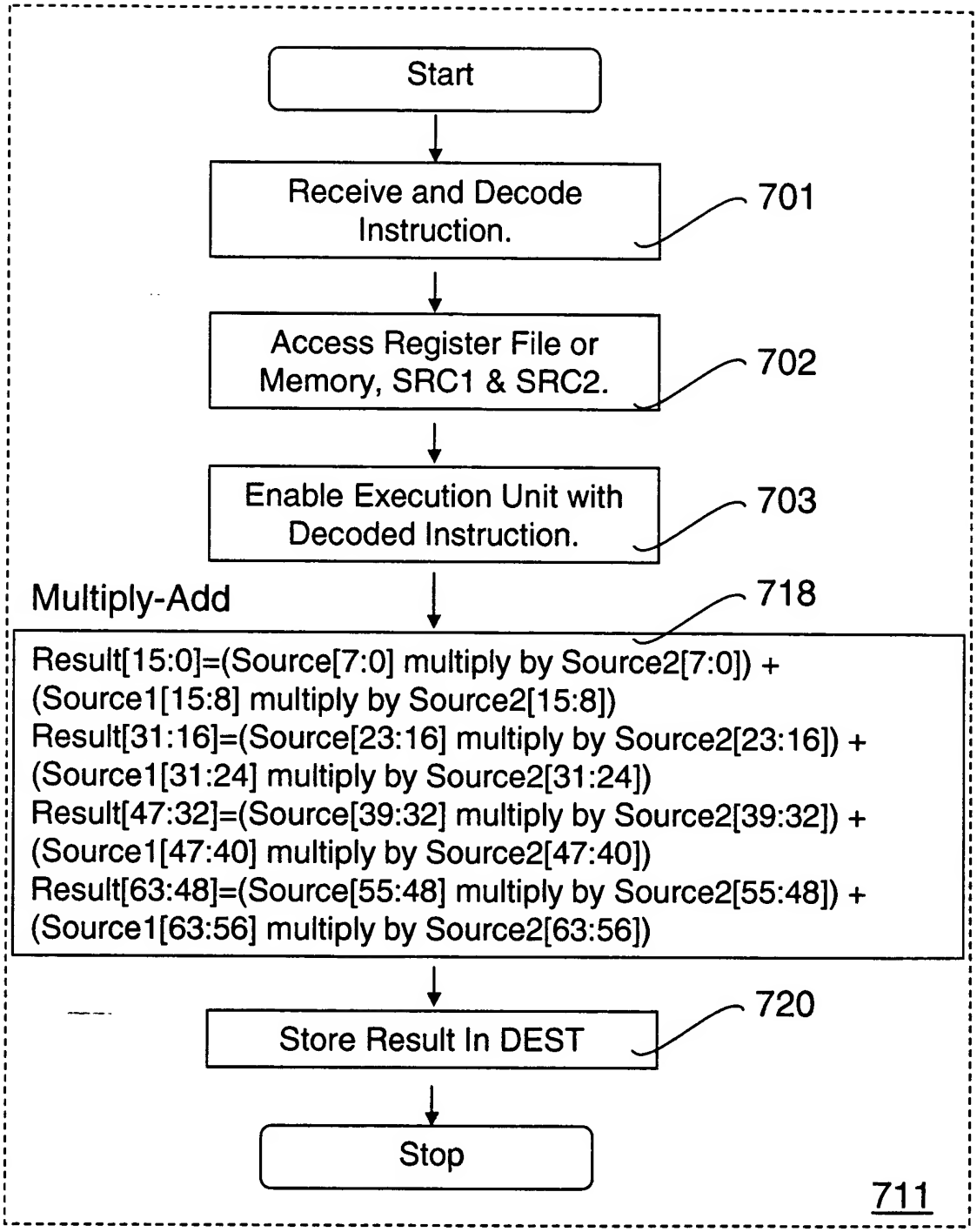

Start
Receive and Decode Instruction.
701
Access Register File or Memory, SRC1 & SRC2.
702
Enable Execution Unit with Decoded Instruction.
703
Multiply-Add
Multiply-Subtract
Result[31:0]=(Source[15:0] multiply by Source2[15:0]) + (Source1[31:16] multiply by Source2[31:16])
Result[63:32]=(Source[47:32] multiply by Source2[47:32]) + (Source1[63:48] multiply by Source2[63:48])
Result[31:0]=(Source[15:0] multiply by Source2[15:0]) - (Source1[31:16] multiply by Source2[31:16])
Result[63:32]=(Source[47:32] multiply by Source2[47:32]) - (Source1[63:48] multiply by Source2[63:48])
714
715
720
Store Result In DEST
Stop
700

FIG. 7b


Start
Receive and Decode Instruction.
701
Access Register File or Memory, SRC1 & SRC2.
702
Enable Execution Unit with Decoded Instruction.
703
Multiply-Add
718
Result[15:0]=(Source[7:0] multiply by Source2[7:0]) + (Source1[15:8] multiply by Source2[15:8])
Result[31:16]=(Source[23:16] multiply by Source2[23:16]) + (Source1[31:24] multiply by Source2[31:24])
Result[47:32]=(Source[39:32] multiply by Source2[39:32]) + (Source1[47:40] multiply by Source2[47:40])
Result[63:48]=(Source[55:48] multiply by Source2[55:48]) + (Source1[63:56] multiply by Source2[63:56])
Store Result In DEST
720
Stop
711

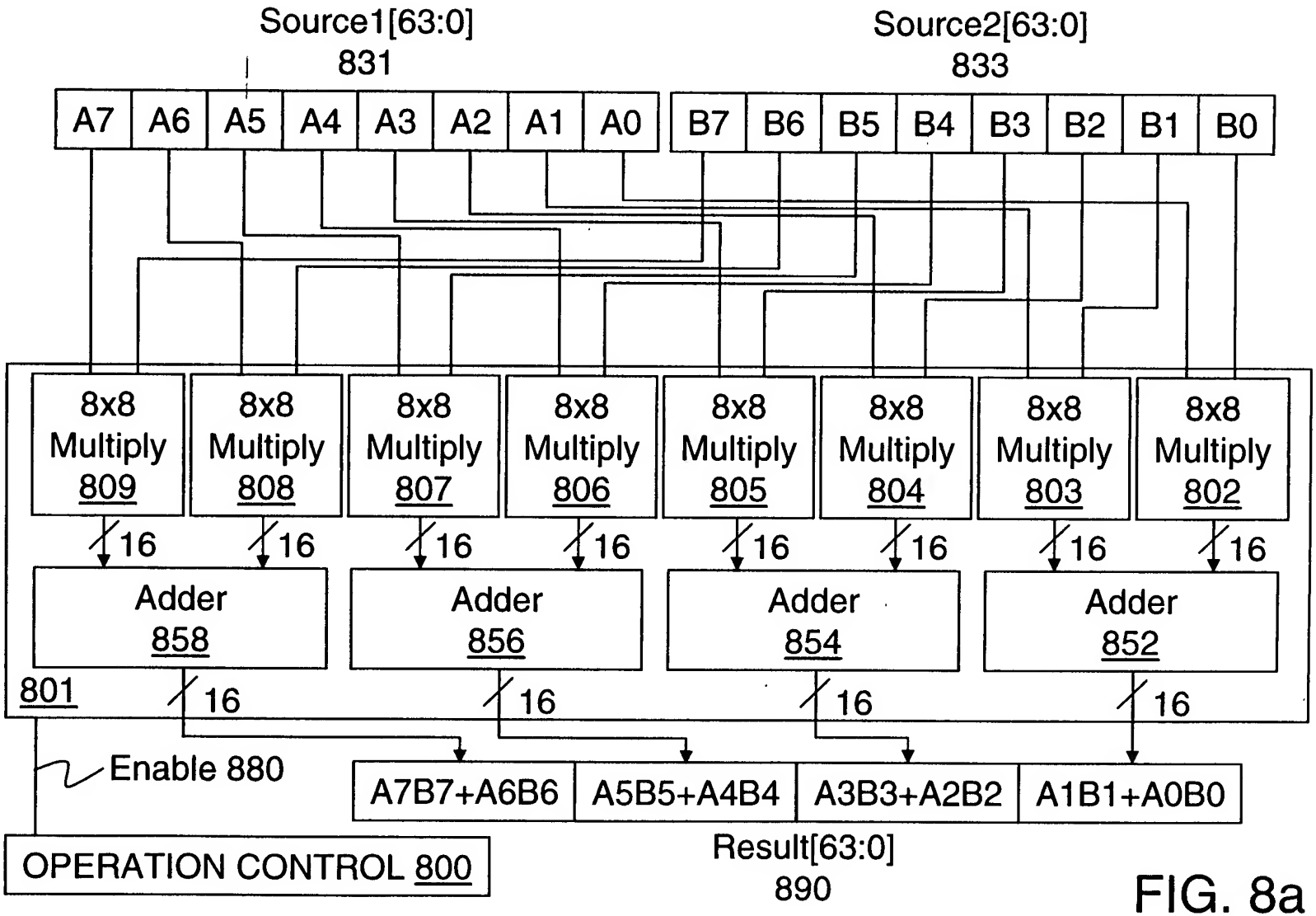

Source1[63:0]
831
Source2[63:0]
833
A7
A6
A5
A4
A3
A2
A1
A0
B7
B6
B5
B4
B3
B2
B1
B0
8x8 Multiply 809
8x8 Multiply 808
8x8 Multiply 807
8x8 Multiply 806
8x8 Multiply 805
8x8 Multiply 804
8x8 Multiply 803
8x8 Multiply 802
16
Adder 858
Adder 856
Adder 854
Adder 852
801
Enable 880
A7B7+A6B6
A5B5+A4B4
A3B3+A2B2
A1B1+A0B0
OPERATION CONTROL 800
Result[63:0]
890

FIG. 8a

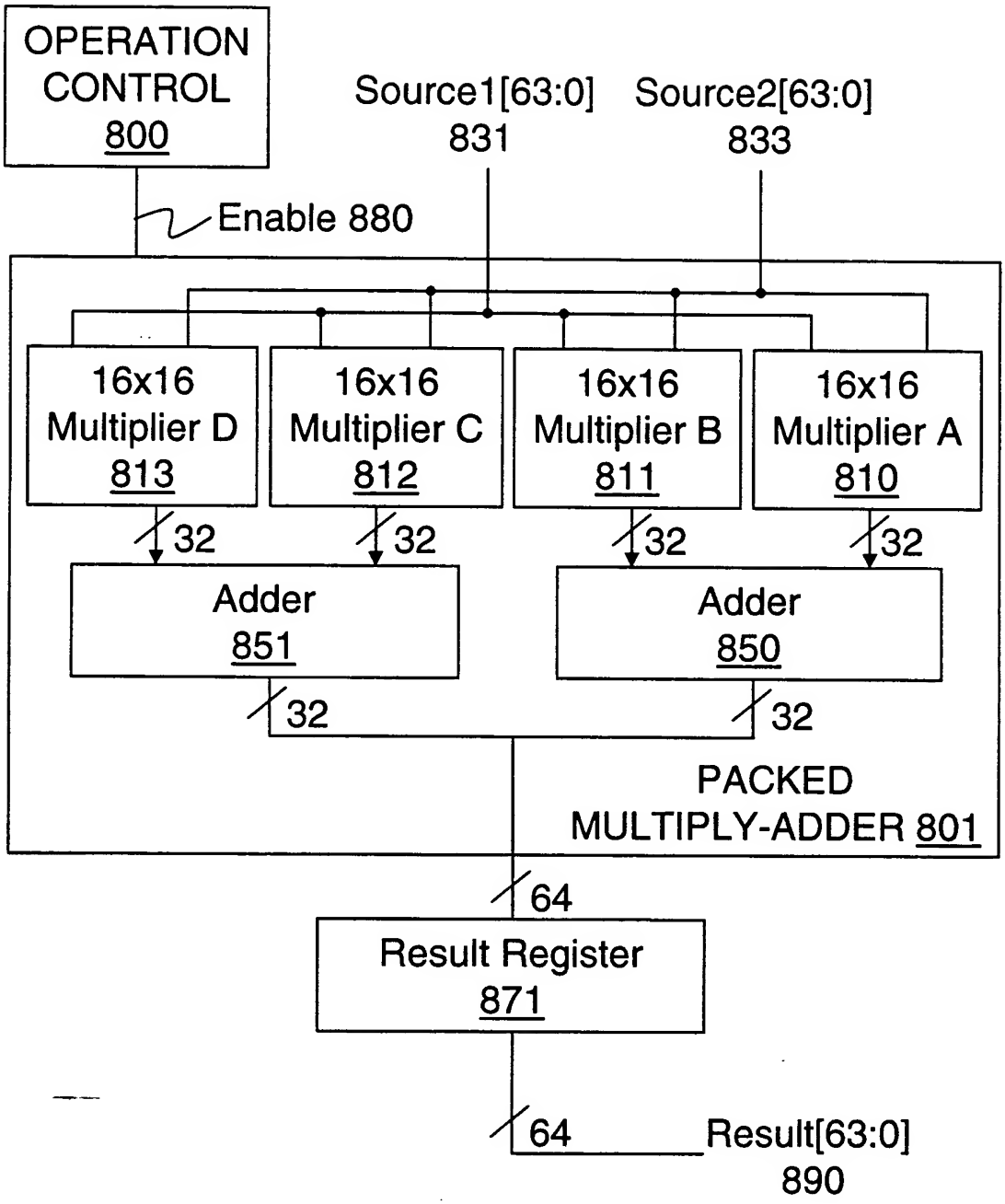

OPERATION CONTROL 800
Source1[63:0] 831
Source2[63:0] 833
Enable 880
16x16 Multiplier D 813
16x16 Multiplier C 812
16x16 Multiplier B 811
16x16 Multiplier A 810
32
32
32
32
Adder 851
Adder 850
32
32
PACKED MULTIPLY-ADDER 801
64
Result Register 871
64
Result[63:0] 890

FIG. 8b

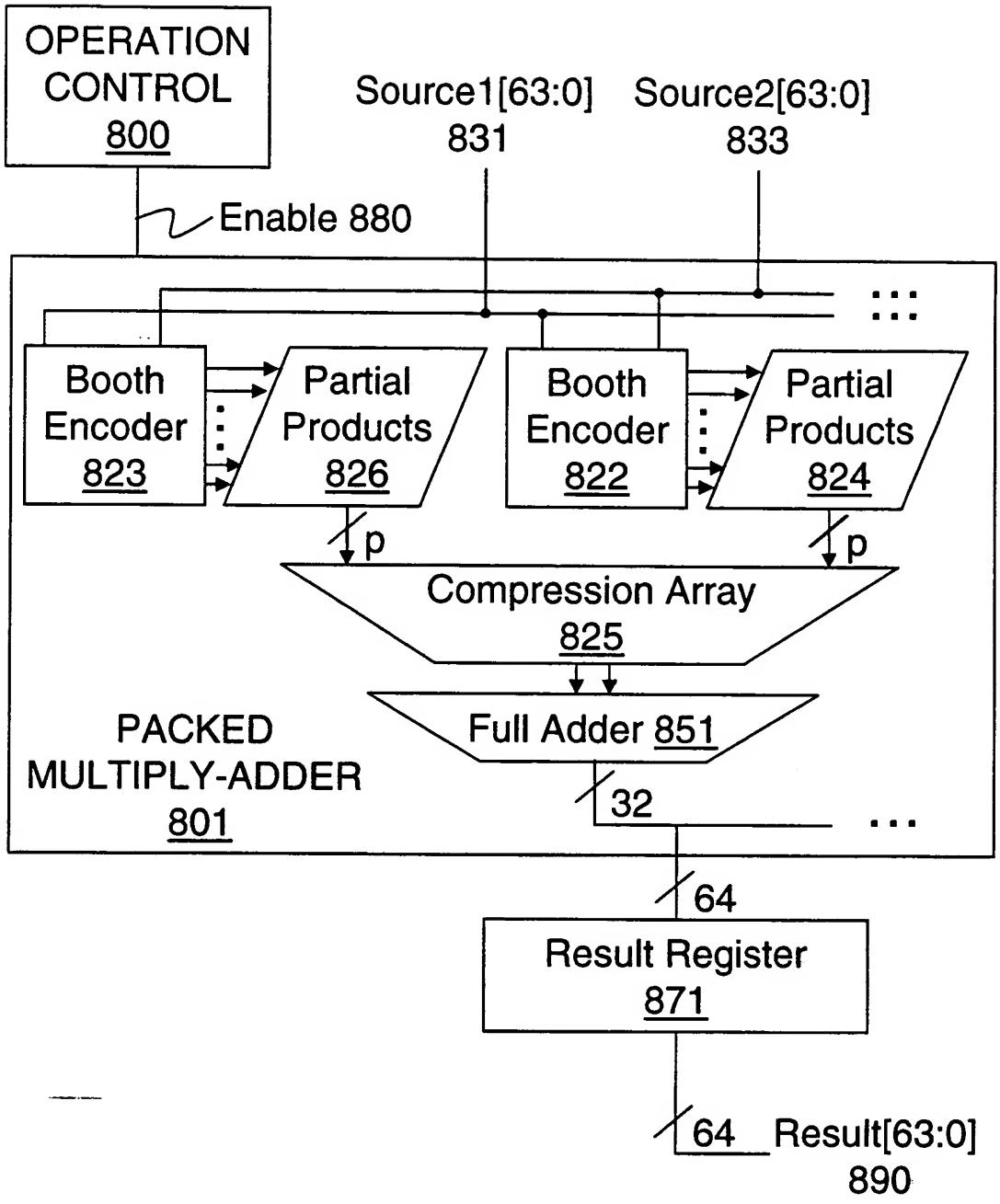

OPERATION CONTROL 800
Source1[63:0] 831
Source2[63:0] 833
Enable 880
Booth Encoder 823
Partial Products 826
Booth Encoder 822
Partial Products 824
p
p
Compression Array 825
Full Adder 851
PACKED MULTIPLY-ADDER 801
32
64
Result Register 871
64
Result[63:0] 890

FIG. 8c

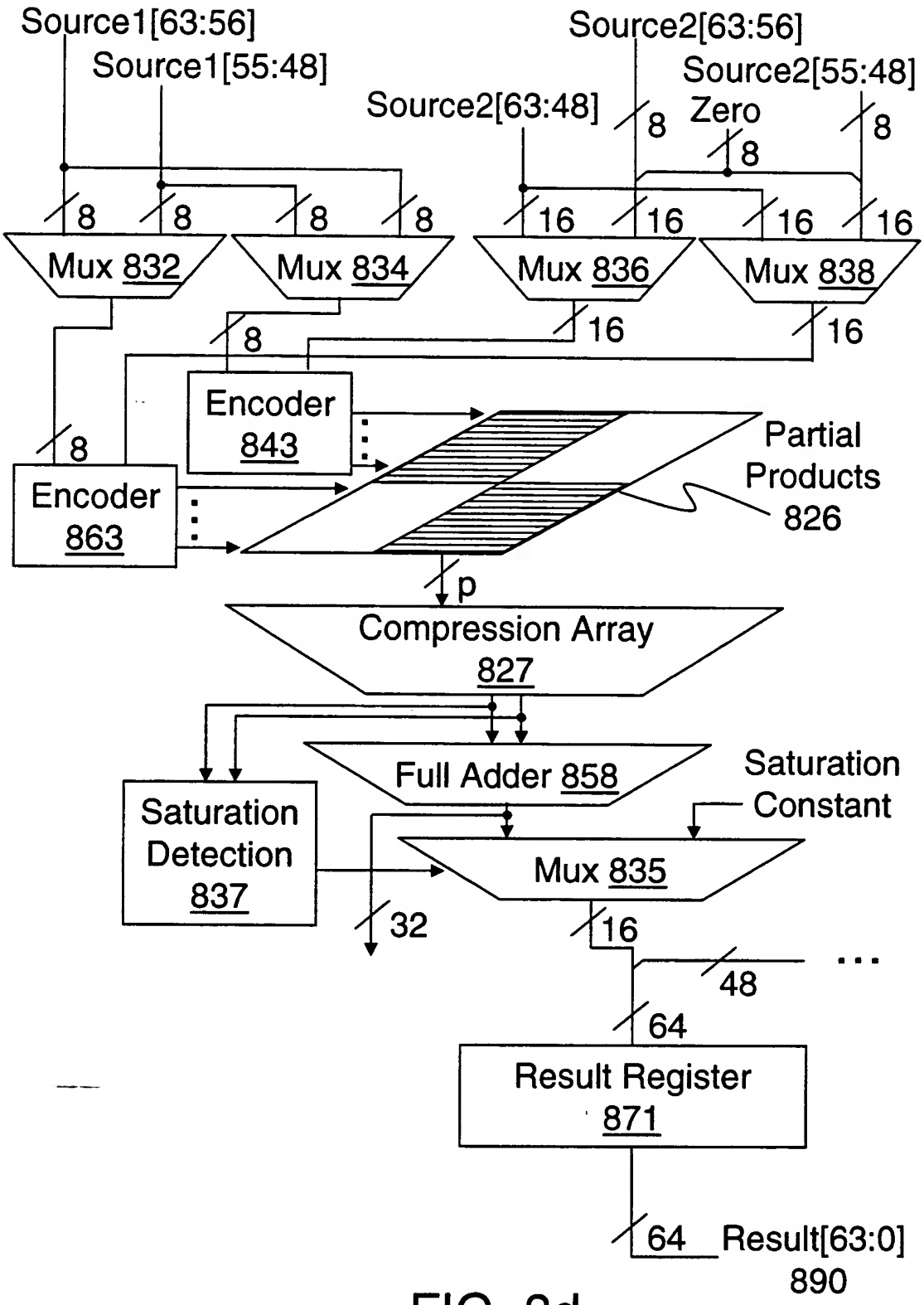

Source1[63:56]
Source1[55:48]
Source2[63:56]
Source2[55:48]
Source2[63:48]
Zero
8
16
Mux 832
Mux 834
Mux 836
Mux 838
Encoder 843
Encoder 863
Partial Products 826
p
Compression Array 827
Full Adder 858
Saturation Constant
Saturation Detection 837
Mux 835
32
48
64
Result Register 871
Result[63:0] 890

FIG. 8d

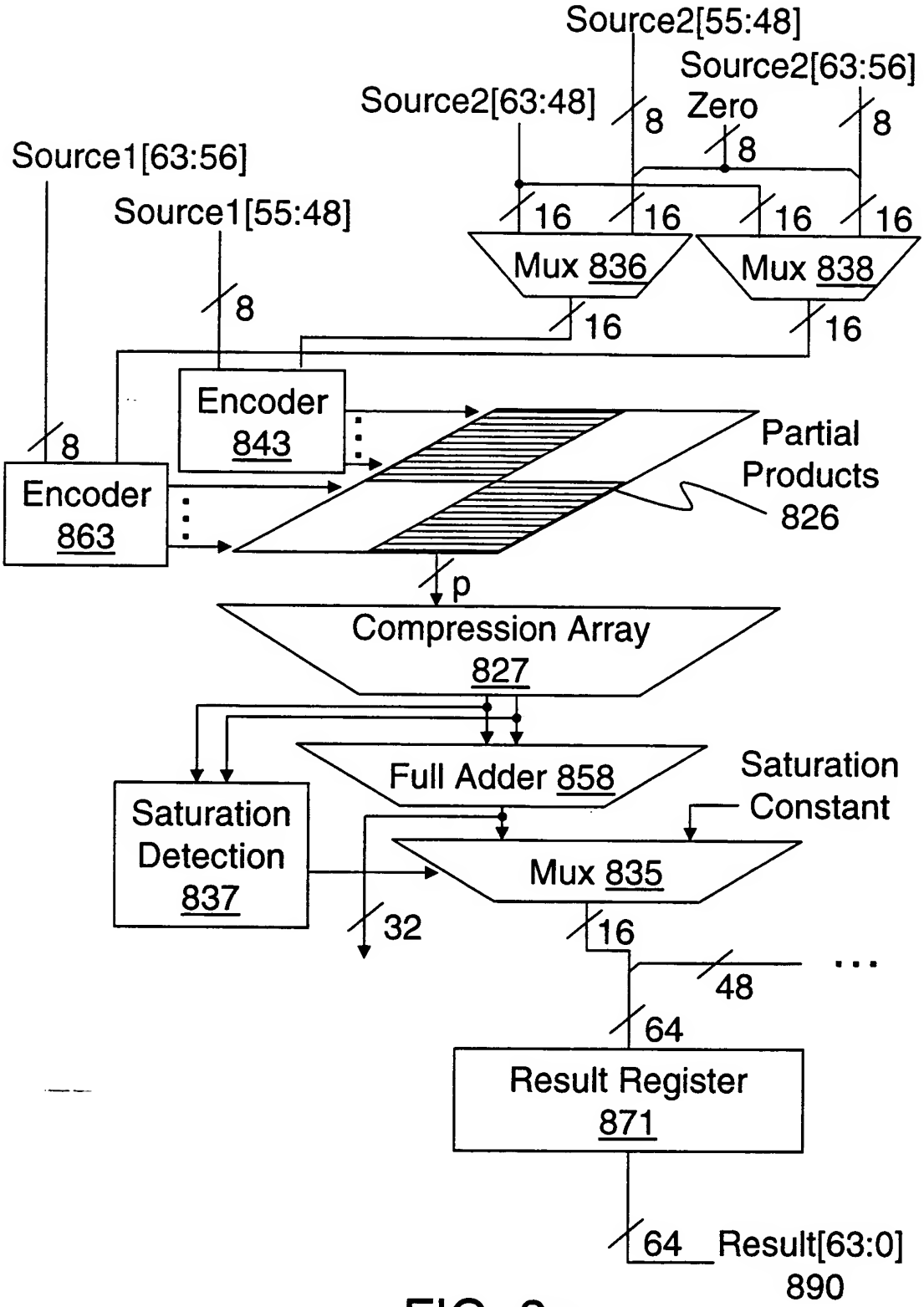

Source2[55:48]
Source2[63:56]
Source2[63:48]
8
Zero
8
8
Source1[63:56]
Source1[55:48]
16
16
16
16
Mux 836
Mux 838
8
16
16
Encoder
843
8
Encoder
863
Partial
Products
826
p
Compression Array
827
Full Adder 858
Saturation
Constant
Saturation
Detection
837
Mux 835
32
16
48
64
Result Register
871
64
Result[63:0]
890

FIG. 8e